Application No.: 09/496,516
Amendment dated: July 9, 2003
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SAR-12165A

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 - 14. (Canceled)

15. (Original) An integrator comprising:

receiving means for receiving a first signal including a first data value and a second data value different from the first data value;

counter means for increasing a count value when the first signal includes the first data value and decreasing the count value when the first signal includes the second data value;

data means for producing a third data value when the count value is equal to or greater than a first threshold value and a fourth data value when the count value is equal to or less than a second threshold value; and

signal generating means for producing a second signal including the third data value and the fourth data value.

16. (Original) The integrator according to claim 15 further comprising a low pass filter comprising the counter means, the data means, and the signal generating means.

17. (Original) The integrator according to claim 15 wherein the counter means includes means for preventing the count value from exceeding a maximum value which is greater than or equal to the first threshold value.

18. (Original) The integrator according to claim 15 wherein the counter means includes means for preventing the count value from exceeding a minimum value which is less than or equal to the second threshold value.

19. (Original) A discriminator comprising:

receiving means for receiving a first signal including a first data value and a second data value different from the first data value;

counter means for increasing a count value when the first signal includes the first data value and resetting the count value to a predetermined value when the first signal includes the second data value; and

clock synchronization means for producing a clock synchronization signal when the count value is equal to or greater than a first threshold value.

20. (Currently Amended) The discriminator according to claim ~~17~~ 19 further comprising data means for producing a third data value when the count value is equal to or greater than the first threshold value and a fourth data value when the count value is reset.

21. (Currently Amended) The ~~integrator~~ discriminator according to claim 19 wherein the counter means includes means for preventing the count value from exceeding a maximum value which is greater than or equal to the first threshold value.

22. (Original) A decoder comprising:

an integrator including:

(a) receiving means for receiving a first signal including a first data value and a second data value different from the first data value,

(b) first counter means for increasing a first count value when the first signal includes the first data value and decreasing the first count value when the first signal includes the second data value,

(c) data means for producing a third data value when the first count value is equal to or greater than a first threshold value and a fourth data value when the first count value is equal to or less than a second threshold value, and

(d) signal generating means for producing a second signal including the third data value and the fourth data value; and

a discriminator including:

(a) second counter means for increasing a second count value when the second signal includes the third data value and resetting the second count value to a predetermined value when the second signal includes the fourth data value, and

(b) clock synchronization means for producing a clock synchronization signal when the second count value is equal to or greater than a third threshold value.

23. (Original) The decoder according to claim 22 further comprising data means for producing third signal including a fifth data value when the count value is equal to or greater than the first threshold value and a sixth data value when the count value is reset.

24. (Original) The decoder according to claim 23 further comprising decoding means for decoding the first signal in response to the third signal and the clock synchronization means.